

Fill the Void

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ABSTRACT

Voids in solder joints are a concern for many electronic manufacturers. They create weakness in the solder joints which can lead to mechanical failure. Voids can slow or limit heat transfer away from the component which can lead to thermal failure. Voids can also interfere with electrical signal flow creating problems with the function of the circuit board. Minimization of voiding is beneficial for the life and function of the circuit assembly.

Voids are caused by many things. Via holes in pads can cause solder paste to flow away from the solder joint creating voids. Gases from via holes can move upwards into the solder joint creating voids. Incomplete wetting or flow of the solder paste can create gaps or voids in the solder joint. Gasses from solder paste fluxes can be trapped in the solder joint. Regardless of the cause of voids there are ways to minimize voiding.

Several methods of minimizing voids are presented in this paper. Stencil design can have a dramatic impact on voiding. Printing solder paste with gas escape routes is an excellent way to reduce voiding. When via in pad designs are used, voiding can be minimized by printing solder paste with a clearance around the via holes. Changes to the reflow profile can help reduce voiding, but the changes need to fit the solder paste. Adding a soak to the reflow profile can drive off volatile materials from certain solder pastes. Lengthening the time above liquidus helps volatile materials to escape from other solder pastes. The solder paste flux has a large influence on voiding. Some solder pastes have a lower potential for voiding than others. A test matrix was designed to validate these methods of minimizing voiding. Void measurements were taken, the data was summarized and a set of recommendations were made. This was all done in an effort to help the reader to "Fill the Void."

Key words: voids, solder joint, stencil design, reflow profile, solder paste

INTRODUCTION

Voids are gaps in a solder joint where the solder does not fill the space between the component and circuit board completely (Figure 1).

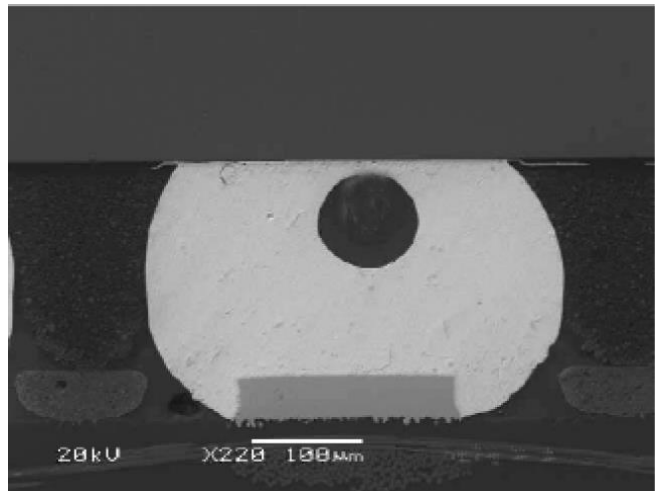


Figure 1: Cross section of a void in a solder joint [1].

Voids can be caused by a variety of things. Often voids are created by the interaction between multiple factors (Figure 2).

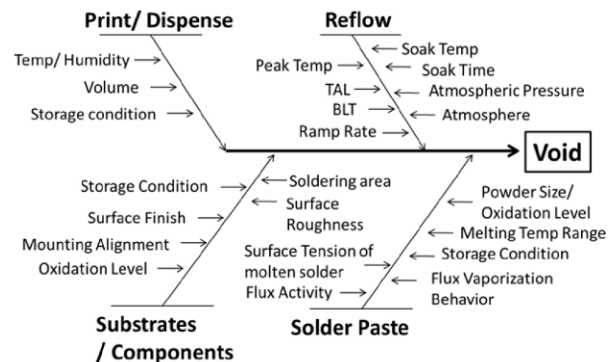


Figure 2: Factors That Influence Voiding [1].

A few of these factors were chosen to be evaluated in this study; solder paste, stencil design and reflow profile. Two different lead-free water soluble solder pastes were chosen

for this evaluation. Solder paste A is a low voiding solder paste and Solder paste B is relatively higher in voiding. The stencil design can have a dramatic effect on voiding. In this study, quad flat no lead (QFN) components were chosen because the solder joint of the thermal pad is known to display voiding. The stencil design for the QFN ground pad was varied using 4 different popular designs. The reflow profile is also known to have a dramatic effect on voiding. Two reflow profiles were used in this study; a standard ramp to spike (RTS) profile and a RTS profile with a higher peak temperature and longer time above liquidus (RTS-HT). The effects of all of these factors on voiding was compared and contrasted.

EXPERIMENTAL METHODOLOGY

This experiment uses a test circuit board called F2A (Figure 3). This circuit board is made of FR4 with etched copper pads that have an electroless nickel - immersion gold surface finish.

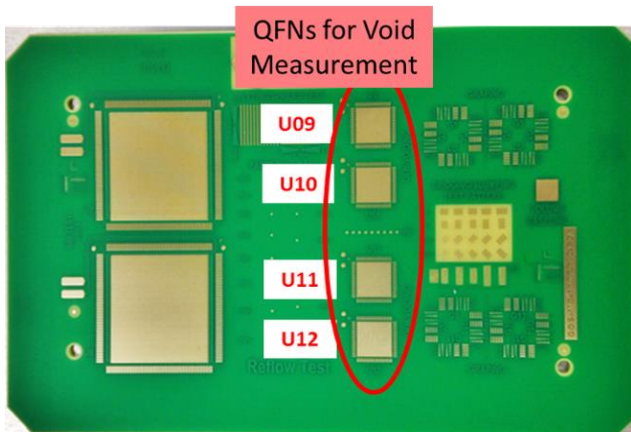


Figure 3: F2A Reflow Test board

This F2A test board has 4 QFN placements per board which were used to measure voiding. From top to bottom these locations are designated as U9, U10, U11, and U12. The components used were 68 lead dummy QFNs with a 100% tin finish. The body size is 10 mm and the lead pitch is 0.5 mm.

The two solder pastes that were used are both water soluble lead free products. Both were made with SAC305 IPC Type 3 (25 – 45 μm) solder powder. Solder pastes A and B exhibit different voiding behavior and are good candidates for the purposes of this study.

The stencil design for each QFN location was varied as shown below (Figure 4).

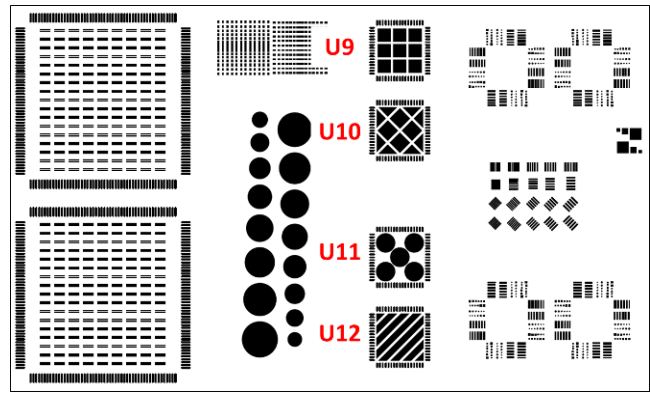


Figure 4: Voiding Stencil Design.

The stencil design at location U9 is a standard window pane. The design at location U10 is a window pane rotated 45 degrees. The stencil design at location U11 is a 5-dot pattern. The design at location U12 is a 45 degree diagonal stripe pattern.

The stencil design details for each QFN location are shown in Table 1. The QFN thermal pad on the circuit board is 327 mils (8.30 mm) square. The stencil was made of 5 mil thick (127 microns) fine grain stainless steel. No nano-coatings were used.

Table 1: Stencil Design for Voiding.

Location	Aperture Shape	Aperture Size in mils (mm)	Spacing in mils (mm)	Paste Coverage Area (%)
U9	Square	88 (2.24)	20 (0.51)	65.3
U10	Diamond	99 (2.51)	20 (0.51)	65.3
U11	Circle	132 (3.35)	8 (0.20)	63.9
U12	Stripe	40 (1.02)	20 (0.51)	65.0

The area of solder paste coverage is close to 65% for each design. The stencil designs were optimized to make this as uniform as possible.

Two different reflow profiles were used. Both profiles were set up in a convection oven with air. The first profile is a standard ramp to spike (RTS) linear profile.

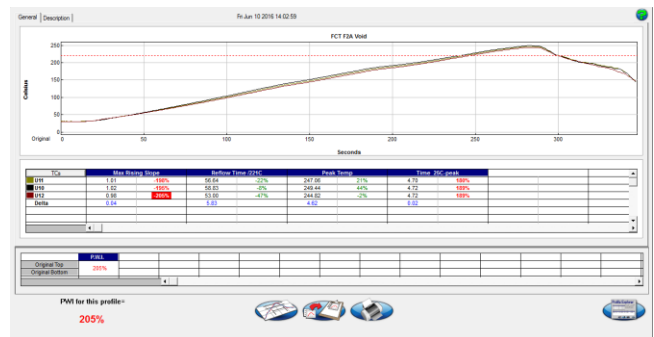


Figure 5: Ramp To Spike (RTS) Profile.

The RTS profile has a time above (TAL) of 53 to 59 seconds and a peak temperature of 245 to 249 °C. The

second profile is a modified RTS profile with a longer time above liquidus and a higher peak temperature (Figure 6).

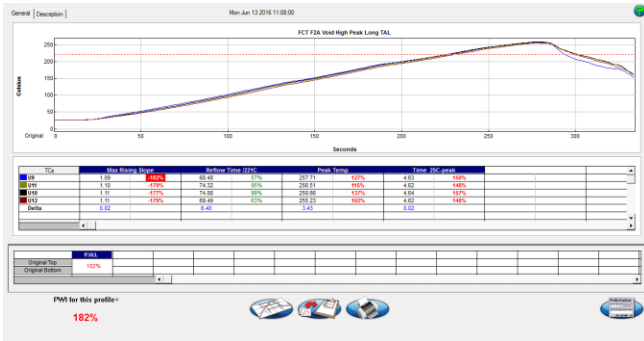


Figure 6: RTS Profile With a Long TAL and High Peak Profile (RTS-HT).

This RTS-HT profile has a TAL of 68 to 75 seconds and a peak temperature of 255 to 259 °C. A summary of these reflow profiles is shown below (Table 2).

Table 2: Reflow Profile Summary.

Setting	RTS Profile	RTS-HT Profile
Ramp rate	0.98 – 1.02 °C/sec	1.09 – 1.10 °C/sec
TAL (>221 °C)	53 – 59 sec	68 – 75 sec
Peak temperature	245 to 249 °C	255 to 259 °C
Profile length (25 °C to peak)	4.70 minutes	4.60 minutes

The X-ray system used to measure voiding was a 2D system that analyzes gray-scale to calculate voiding area. The X-ray source was set to a voltage of 70 kV and a current of 400 μA.

RESULTS

Solder Paste Effects on Voiding

The two water soluble, lead-free solder pastes chosen for this study showed dramatic differences in voiding. The overall average voiding results for these solder pastes is shown below (Figure 7).

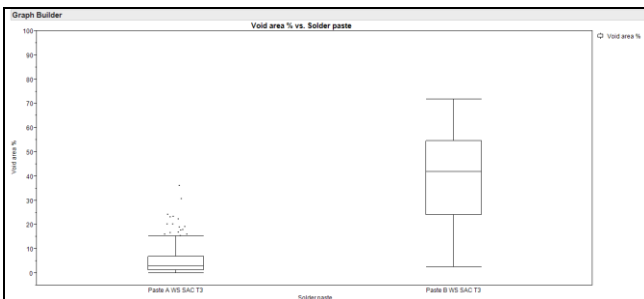


Figure 7: Voiding by Solder Paste.

Solder paste A gave much lower voiding than solder paste B. X-ray images of the voids are shown below (Figure 8).

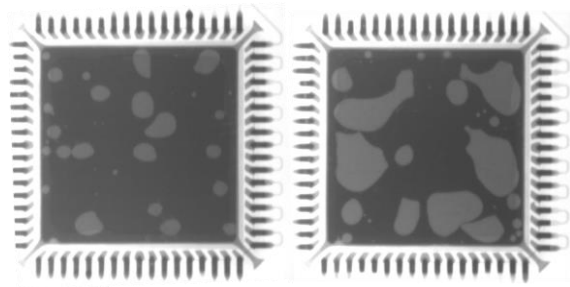


Figure 8: X-Ray Images of Voiding (Solder Paste A – Left, Solder Paste B - Right).

This result is statistically significant as shown by Tukey-Kramer Honest Significant Difference (HSD) testing (Figure 9).

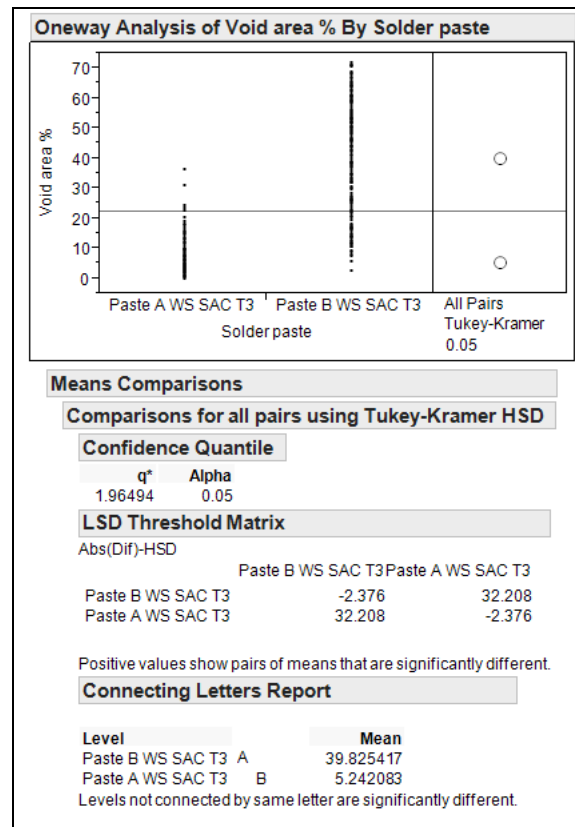


Figure 9: Tukey-Kramer HSD Analysis for Voiding by Solder Paste.

Stencil Design Effects on Voiding

Three of the four different stencil designs generated similar levels of voiding (Figure 10). Slightly higher voiding was found at location U11, which is the 5-dot stencil design.

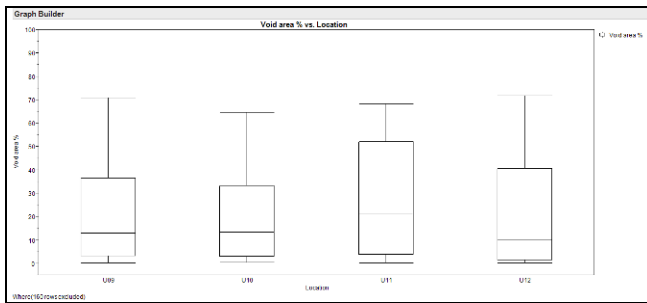


Figure 10: Voiding by Stencil Design.

Representative images of voiding by stencil design are shown below (Figure 11).

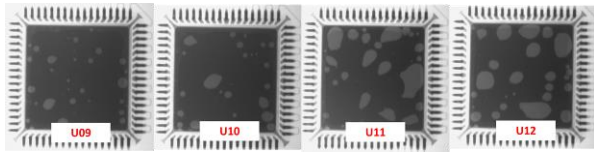


Figure 11: X-Ray Images of Voiding by Stencil Design.

These images show higher voiding with the 5-dot pattern (U11) and the diagonal stripe pattern (U12). The statistics show that the voiding is higher with U11 and the other three designs are fairly similar in voiding levels. This is validated by Tukey-Kramer HSD testing (Figure 12).

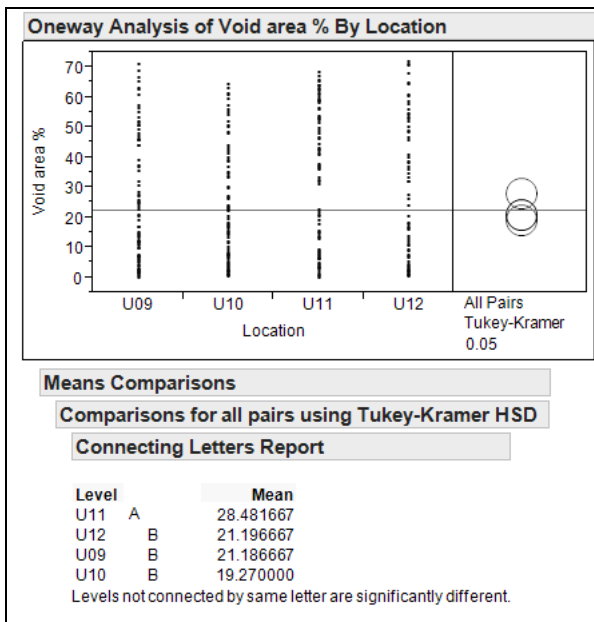


Figure 12: Tukey-Kramer HSD Analysis for Voiding by Stencil Design.

Reflow Profile Effects on Voiding

Two different reflow profiles were used and the voiding results were compared to each other. The voiding results for each are shown below (Figure 13).

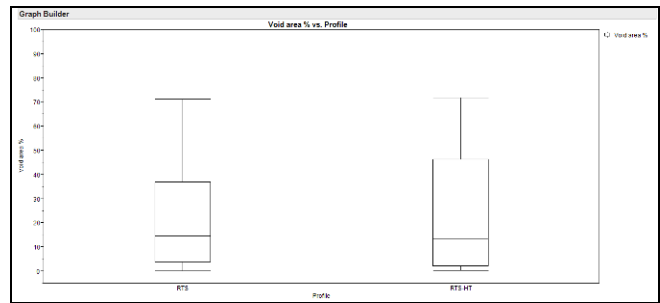


Figure 13: Voiding by Reflow Profile.

The reflow profiles tested did not show a significant difference on voiding across all of the tests performed. This is validated by Tukey-Kramer HSD analysis (Figure 14).

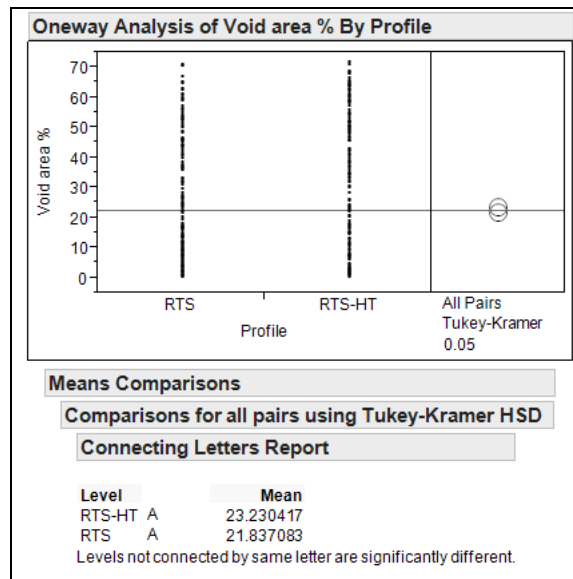


Figure 14: Tukey-Kramer HSD Analysis for Voiding by Reflow Profile.

Multi-Variable Effects on Voiding

Further analysis of this data by multiple variables gave some interesting results. Voiding by stencil design separated by solder paste is shown below (Figure 15).

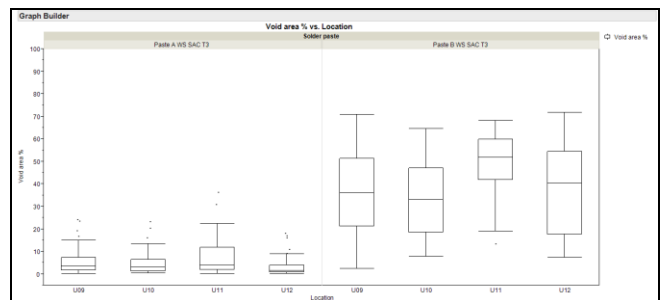


Figure 15: Voiding by Stencil Design Separated by Solder Paste. (Solder Paste A – Left. Solder Paste B - Right).

Tukey-Kramer HSD analysis of this data shows some slight differences in voiding performance between these pastes and stencil designs (Figure 16).

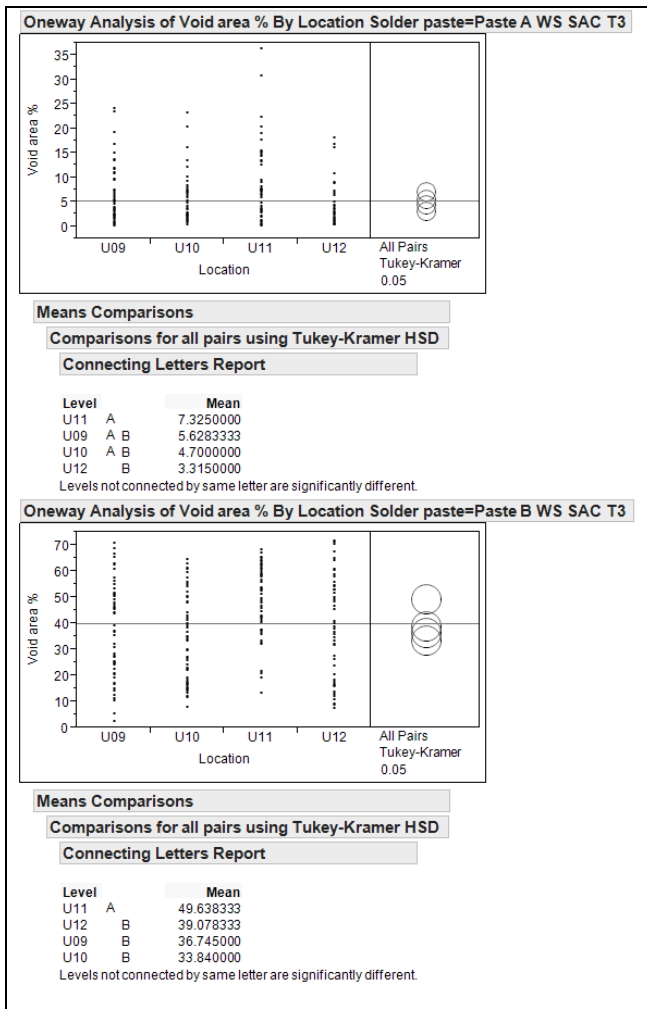


Figure 16: Tukey-Kramer HSD Analysis for Voiding by Stencil Design Separated by Solder Paste.

With solder paste A, the 5-dot stencil design (U11) gave significantly higher voiding than the diagonal stripe design (U12). The other two cross hatch stencil designs (U09 and U10) gave very similar results.

Solder paste B gave different results. The 5-dot stencil design (U11) gave a much higher voiding level than all of the other three stencil designs which were statistically similar.

Voiding by reflow profile separated by solder paste is shown below (Figure 17).

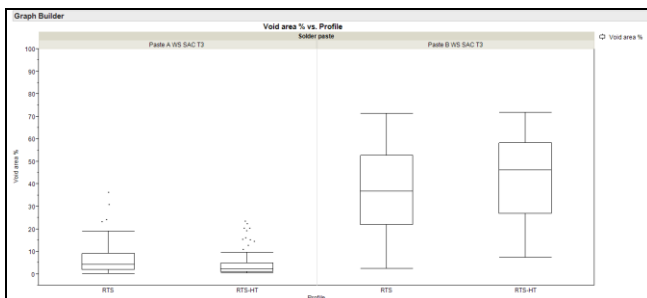


Figure 17: Voiding by Reflow Profile Separated by Solder Paste. (Solder Paste A – Left. Solder Paste B - Right).

Tukey-Kramer HSD analysis shows significant differences in these results (Figure 18).

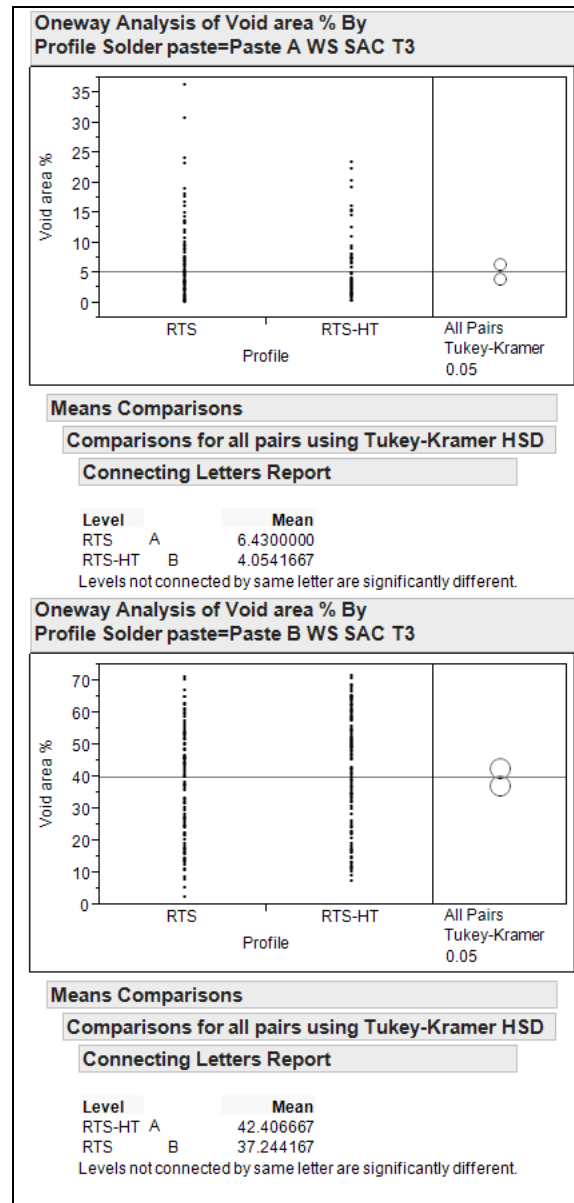


Figure 18: Tukey-Kramer HSD Analysis for Voiding by Reflow Profile Separated by Solder Paste.

The long TAL and high peak profile (RTS-HT) gives lower voiding than the standard linear ramp profile (RTS), with solder paste A. This result is reversed for solder paste B. Solder paste B generates higher voiding with the long TAL and high peak profile than with the standard linear ramp profile. This is a perfect example of how the solder paste and profile must be paired to minimize voiding.

Largest Void Size

It was observed that as void area % increased, the size of the largest void also increased (Figure 19).

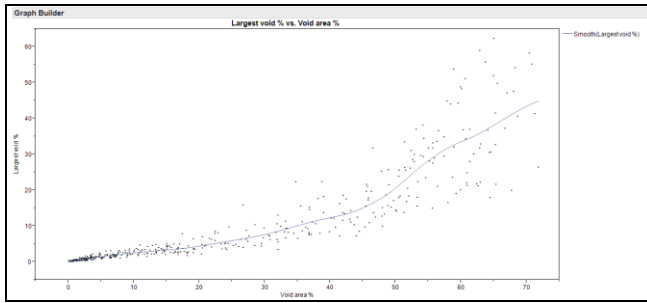


Figure 19: Largest Void % Increases with Increasing Void Area %.

In general, as void area % increases the scatter in the size of the largest void also increases. In other words, the distribution of void size becomes larger as overall voiding increases.

This same trend is true for the solder pastes used. Solder paste B generated higher overall voiding and also generated larger voids (Figure 20).

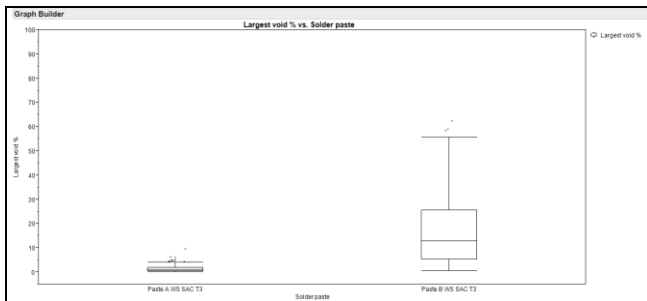


Figure 20: Largest Void Variation by Solder Paste.

This trend can also be seen with the stencil design. The 5-dot stencil design (U11) generated larger voids (Figure 21).

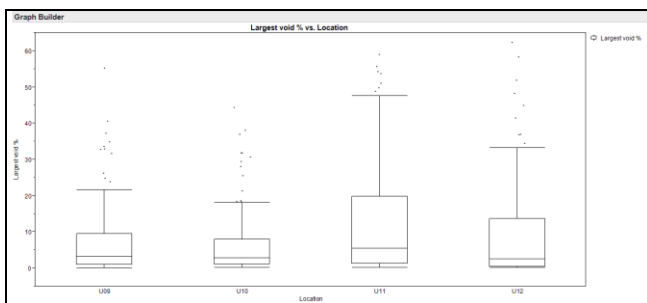


Figure 21: Largest Void Variation by Stencil Design.

Tukey-Kramer HSD analysis shows that the results above are statistically significant.

An interesting result occurred with the largest void size with regards to reflow profile. The overall voiding levels generated by each reflow profile were similar (Figure 13 above). The long TAL – high peak temperature profile seems to have generated larger voids than the ramp to spike profile as shown below (Figure 22).

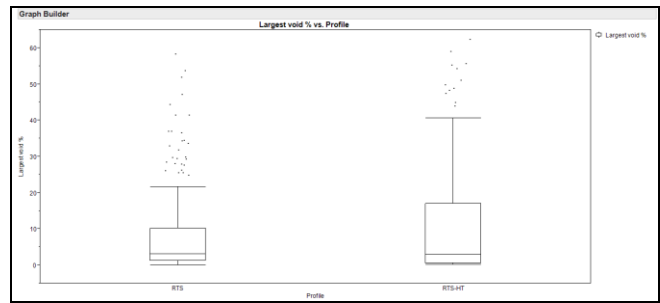


Figure 22: Largest Void Variation by Reflow Profile.

Tukey-Kramer HSD testing shows no significant difference in the largest void sizes generated by the reflow profiles (Figure 23).

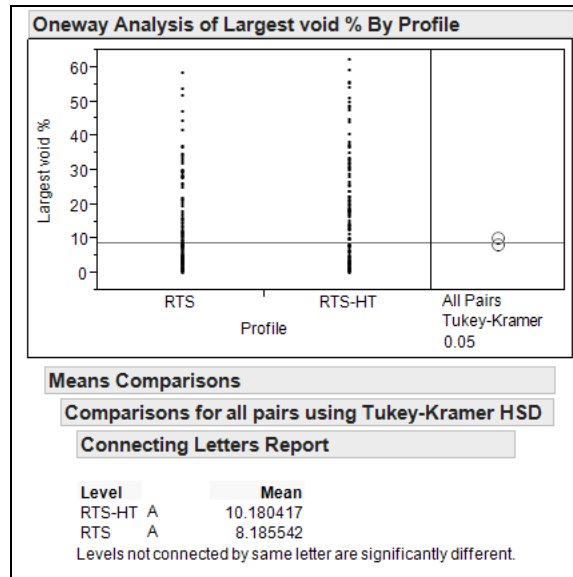


Figure 23: Tukey-Kramer HSD Testing of Largest Void Size by Reflow Profile.

Fill the Void

What have we learned about voiding?

- Solder paste B generated higher overall voiding and larger voids than solder paste A.
- The stencil design of QFN ground pads has some effect on voiding. The 5-dot pattern generated higher voiding and larger voids than the other patterns.
- A standard linear ramp to spike type reflow profile generates higher voiding than a long TAL - high peak temperature profile for solder paste A. This voiding result was reversed for solder paste B.

Based on the results of this work, here are recommendations to help “Fill the Void.”

1. Use a solder paste that generates low voiding in your process. This can have a dramatic effect on voiding.

2. Implement a stencil design to minimize voiding. Use a stencil supplier that can recommend low voiding designs based on lab and field experience.
3. Optimize the reflow profile for the solder paste that is used. The solder paste and reflow profile have to work together to minimize voiding.

CONCLUSIONS

Voiding in solder joints is affected by many factors. As shown in this study, voiding is influenced by the solder paste flux chemistry, the stencil design and the reflow profile used. In this work, there was a clear difference in voiding from one solder paste to the other. The stencil design had a small effect on voiding, although the 5-dot pattern design showed higher voiding than window pane or diagonal stripe patterns. The reflow profiles tested had different effects on voiding for each of the solder pastes. The ramp to spike profile gave lower voiding with solder paste B, while the long time above liquidus – high peak profile gave lower voiding with solder paste A. This shows that the reflow profile must be paired with the solder paste and the stencil design in order to minimize voiding.

Only a small number of factors that influence voiding were studied in this work. There is much more testing to be done. Due to the commonplace use of bottom terminated components, it is clear that voiding will be an issue that many must address. The authors will continue to study factors that influence voiding in an effort to help the reader to “Fill the Void”.

FUTURE WORK

Development of strategies for mitigation of voiding is ongoing and these strategies will be presented in future technical papers. The voiding effects of various no clean solder pastes are being studied. The particle size of the solder powder and the manufacturers of the solder powder are being examined for their effects on voiding. Stencil design optimization is also under investigation. Vapor phase reflow with vacuum is being tested and compared to convection reflow. The possibility of using vapor phase reflow with vacuum to rework solder joints with voids is under investigation. A combination of mitigation strategies can have a dramatic effect on the occurrence of voiding.

ACKNOWLEDGEMENTS

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REFERENCES

[1] K. Sweatman, T. Nishimura, K. Sugimoto, A. Kita, “Controlling Voiding Mechanisms in the Reflow Soldering Process”, Proceedings of IPC APEX Expo, 2016.