

# **FILL THE VOID IV: ELIMINATION OF INTER-VIA VOIDING**

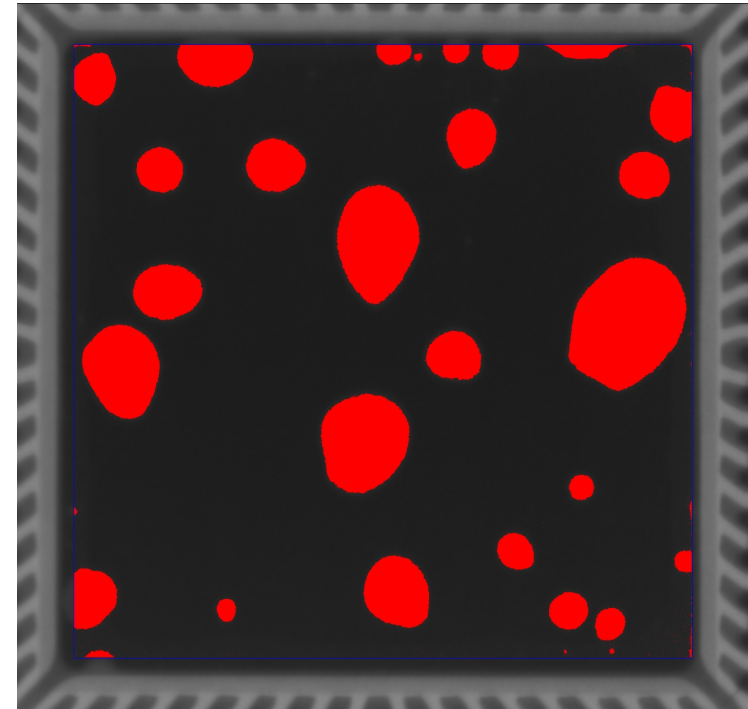
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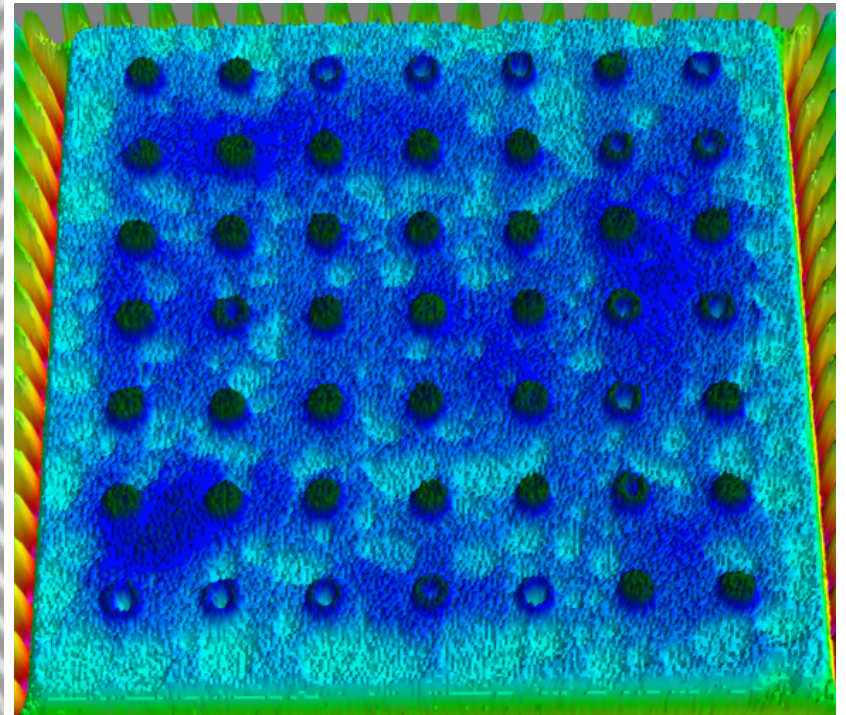
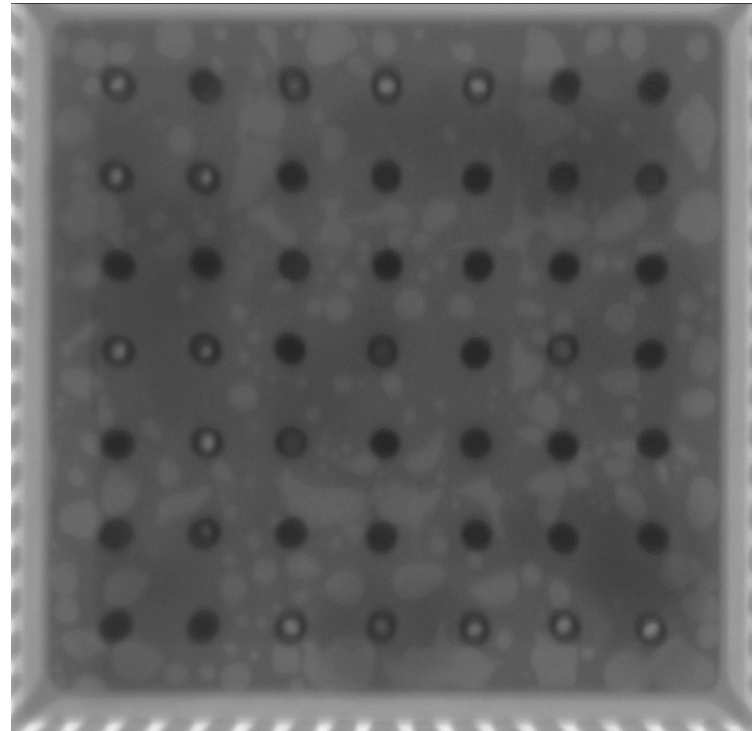
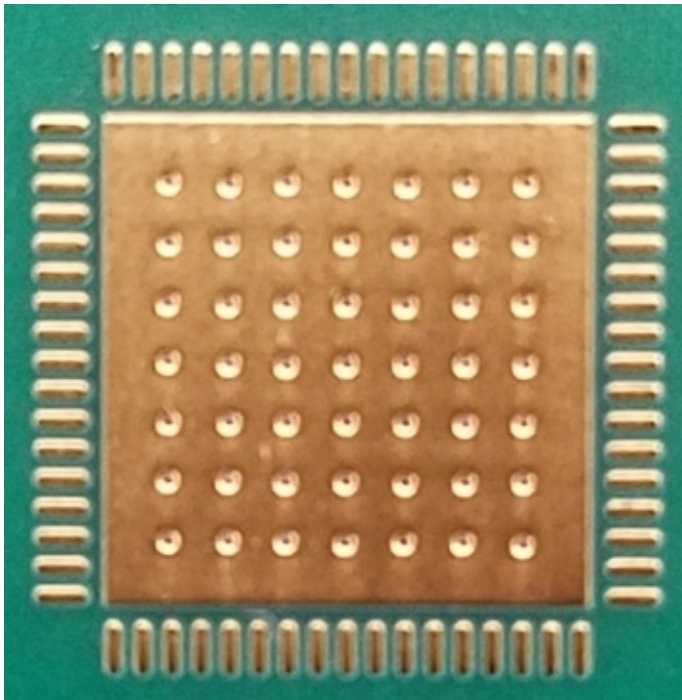
# OUTLINE

- Introduction
- Factors that Influence Voiding
- Methodology
- Voiding Results
- Recommendations to Fill the Void
- Future Work
- Acknowledgements
- Thank You & Questions



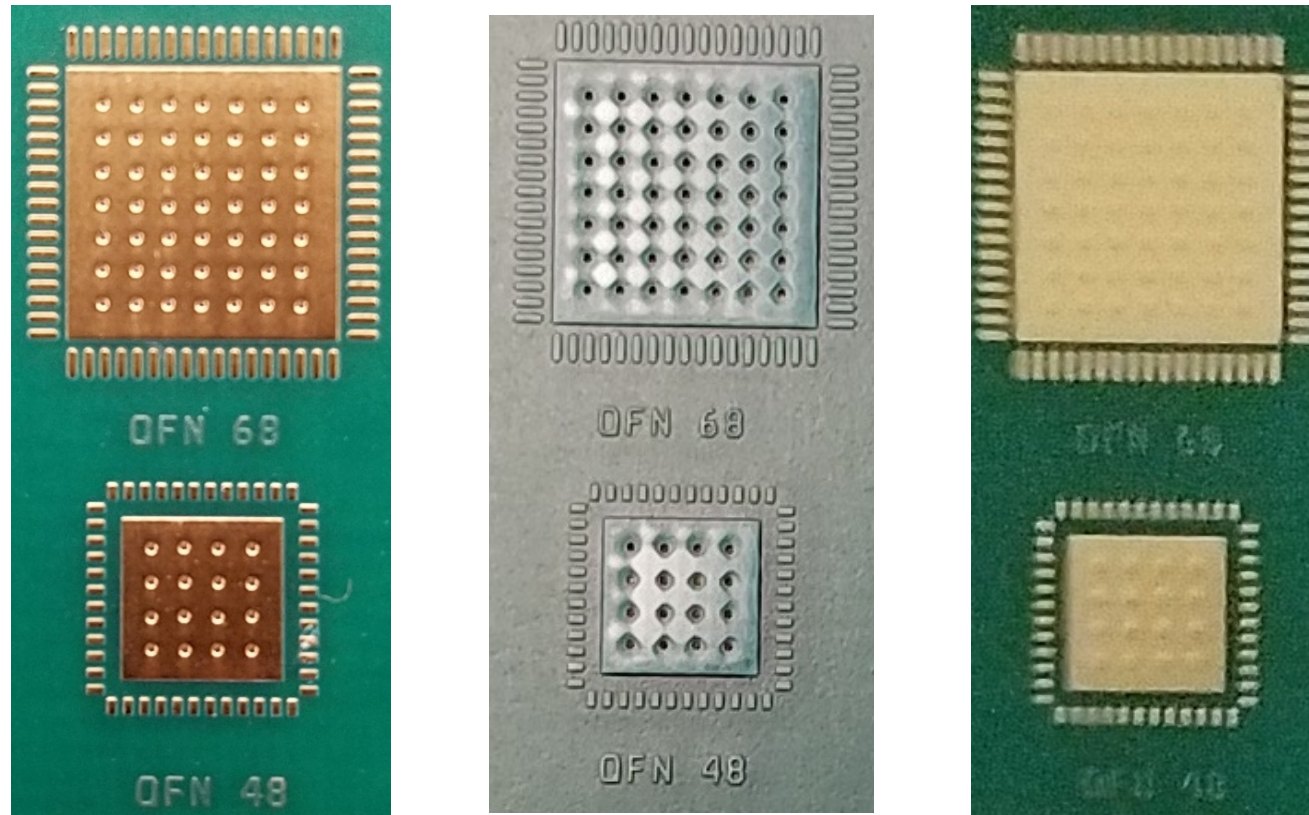
# INTRODUCTION

## INTRODUCTION ON VOIDING



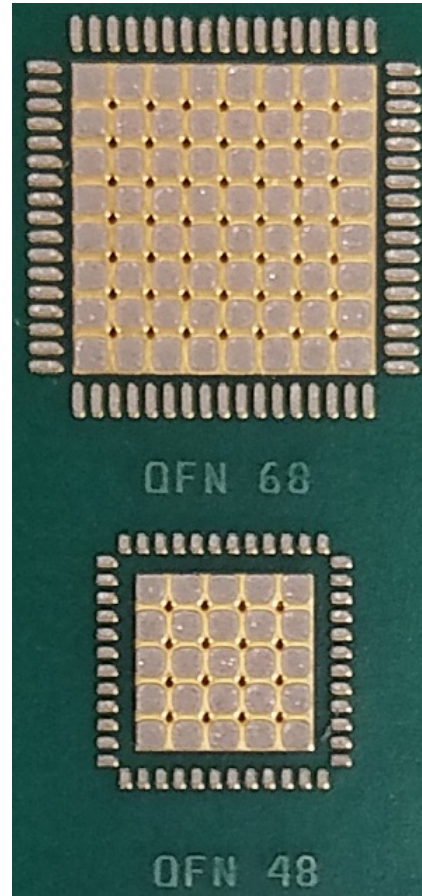
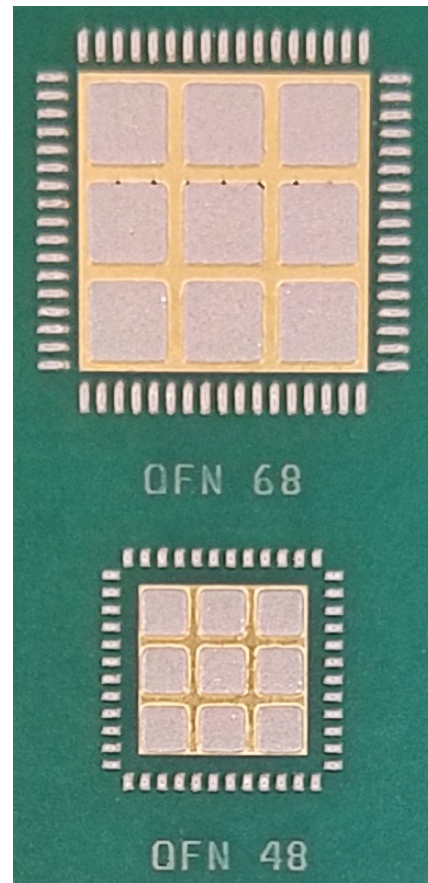
Voiding is Common for QFN Thermal Pads with Via Holes

# FACTORS THAT INFLUENCE VOIDING FOR VIA-IN-PAD DESIGNS



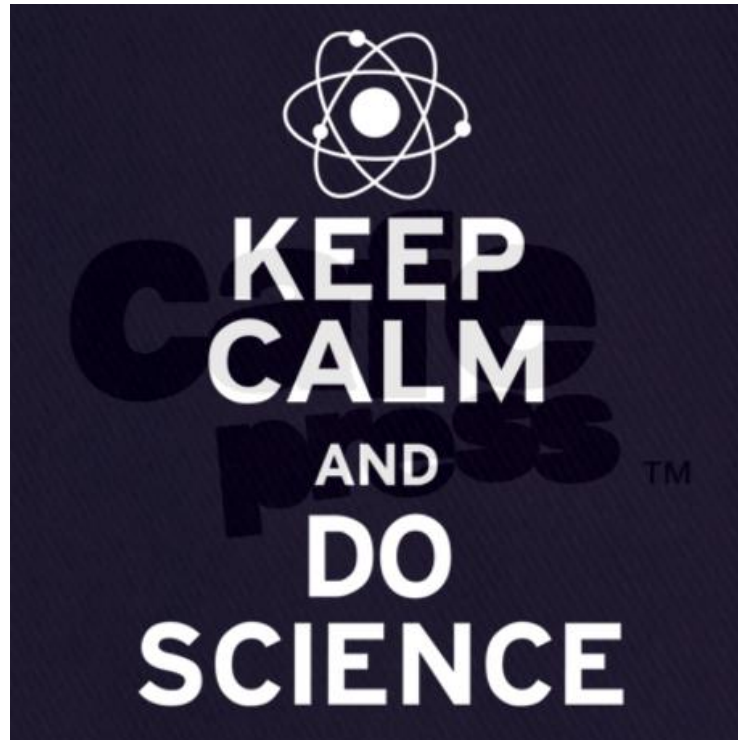
Via Hole Plugging Options: Open, S/M Tent, Plugged

# FACTORS THAT INFLUENCE VOIDING FOR VIA-IN-PAD DESIGNS

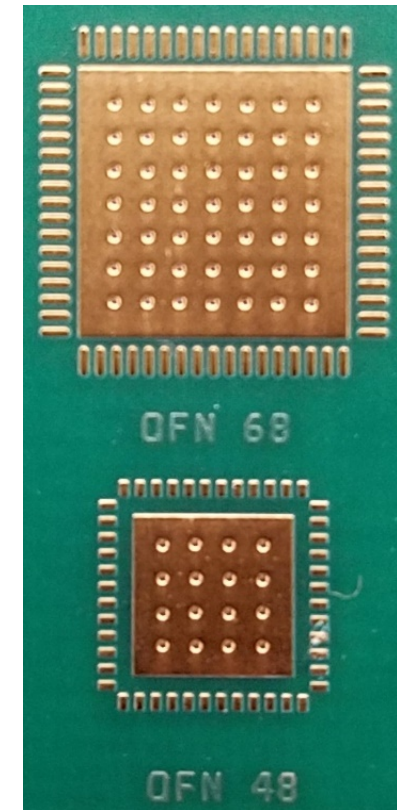
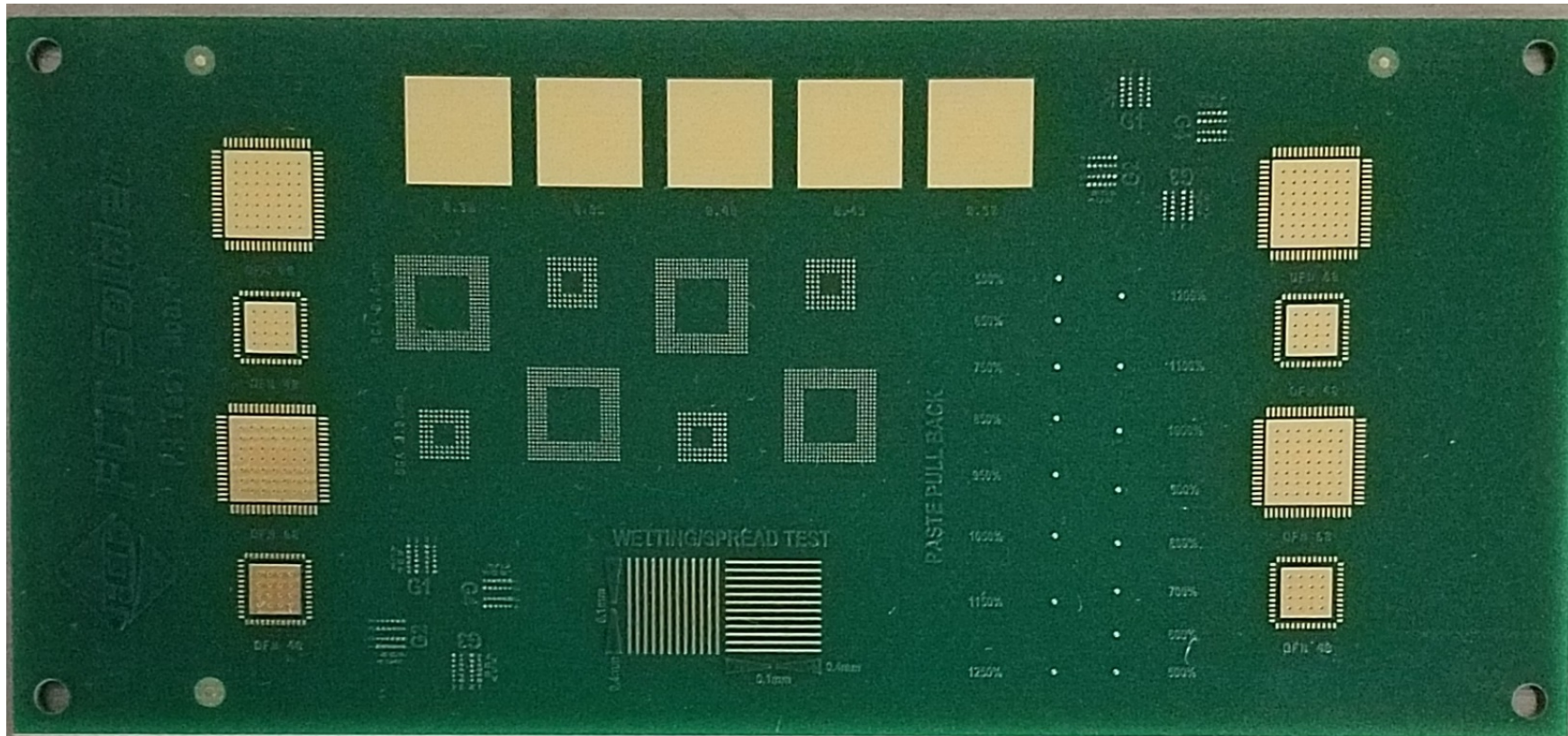


Solder Paste Print Options: Print over Vias, Print around Vias

# METHODOLOGY



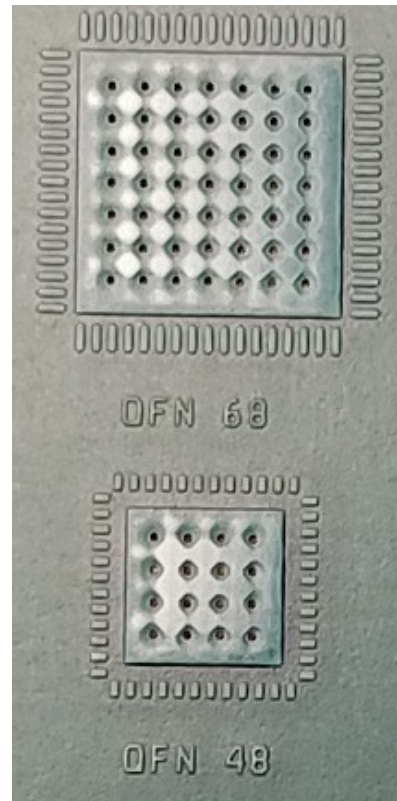
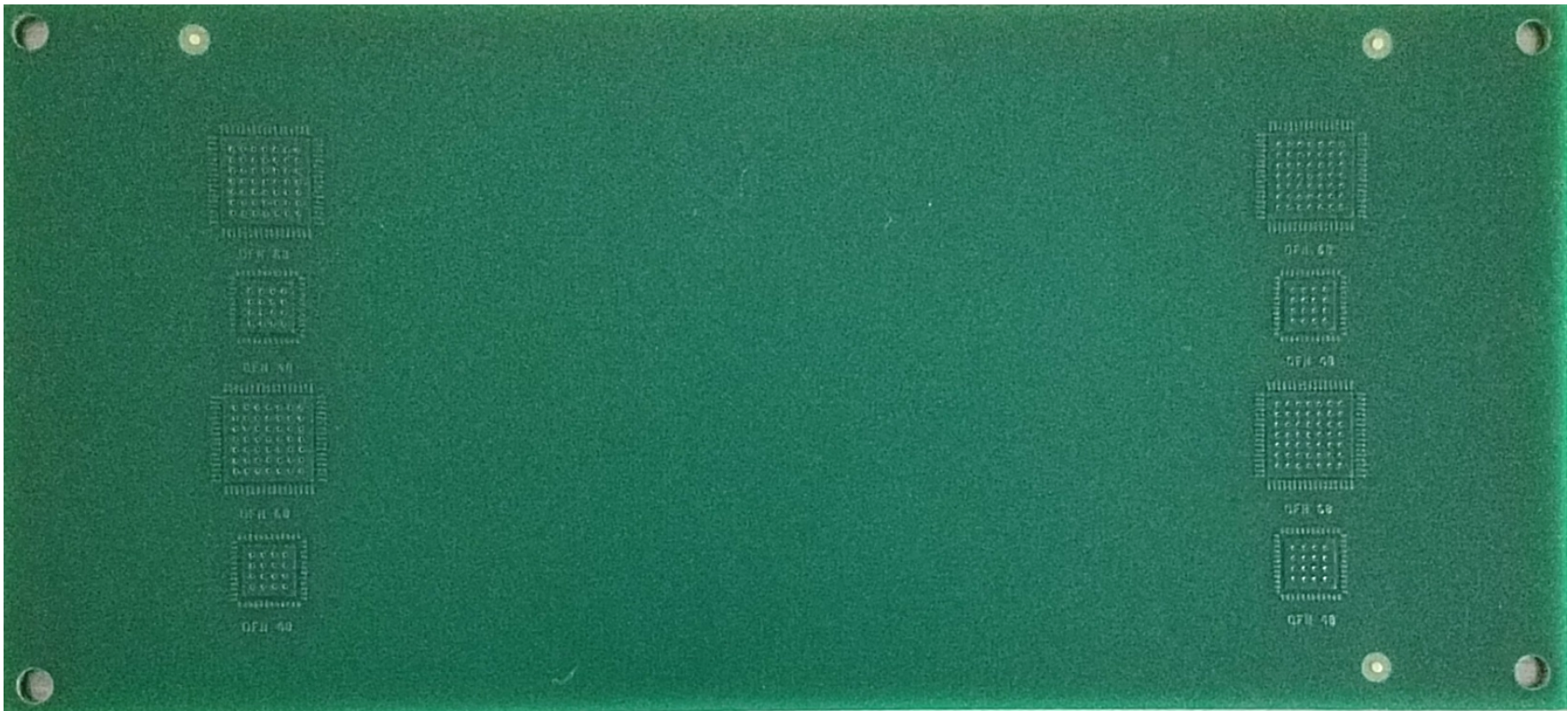
# METHODOLOGY – CIRCUIT BOARDS



PR Test Board with Via in Pad (0.3 mm = 12 mil vias), Plated with ENIG

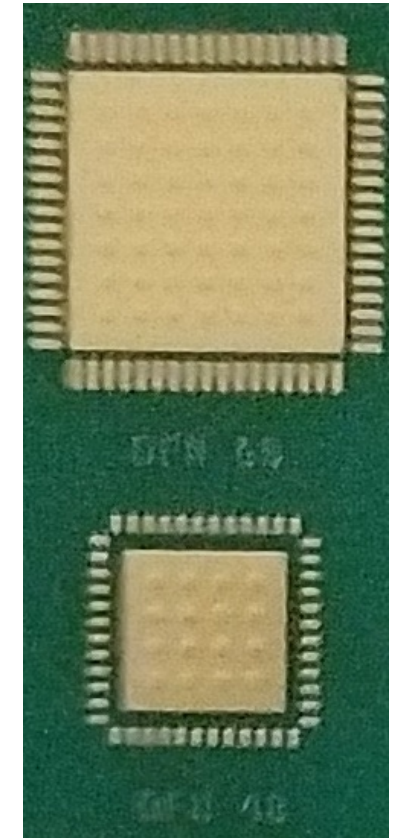
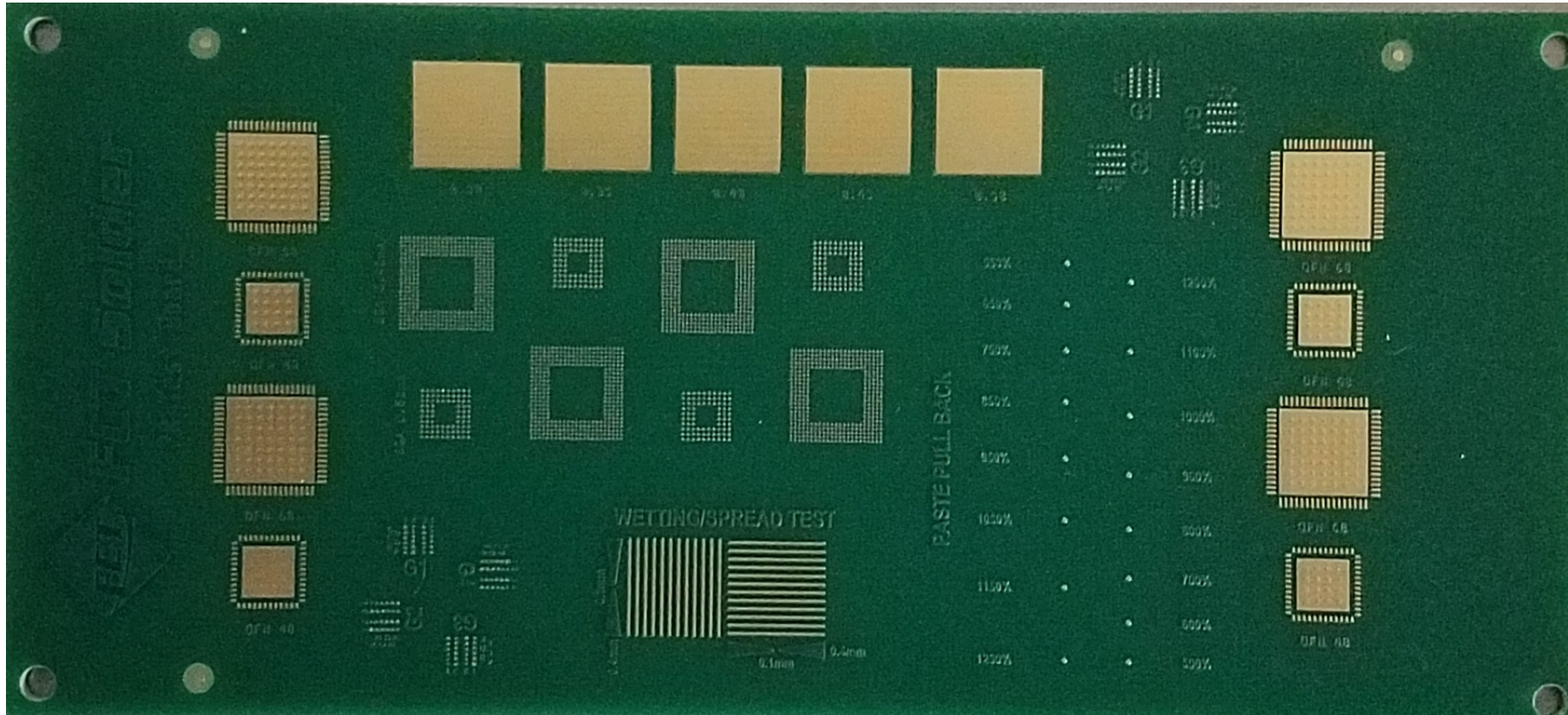


# METHODOLOGY – CIRCUIT BOARDS



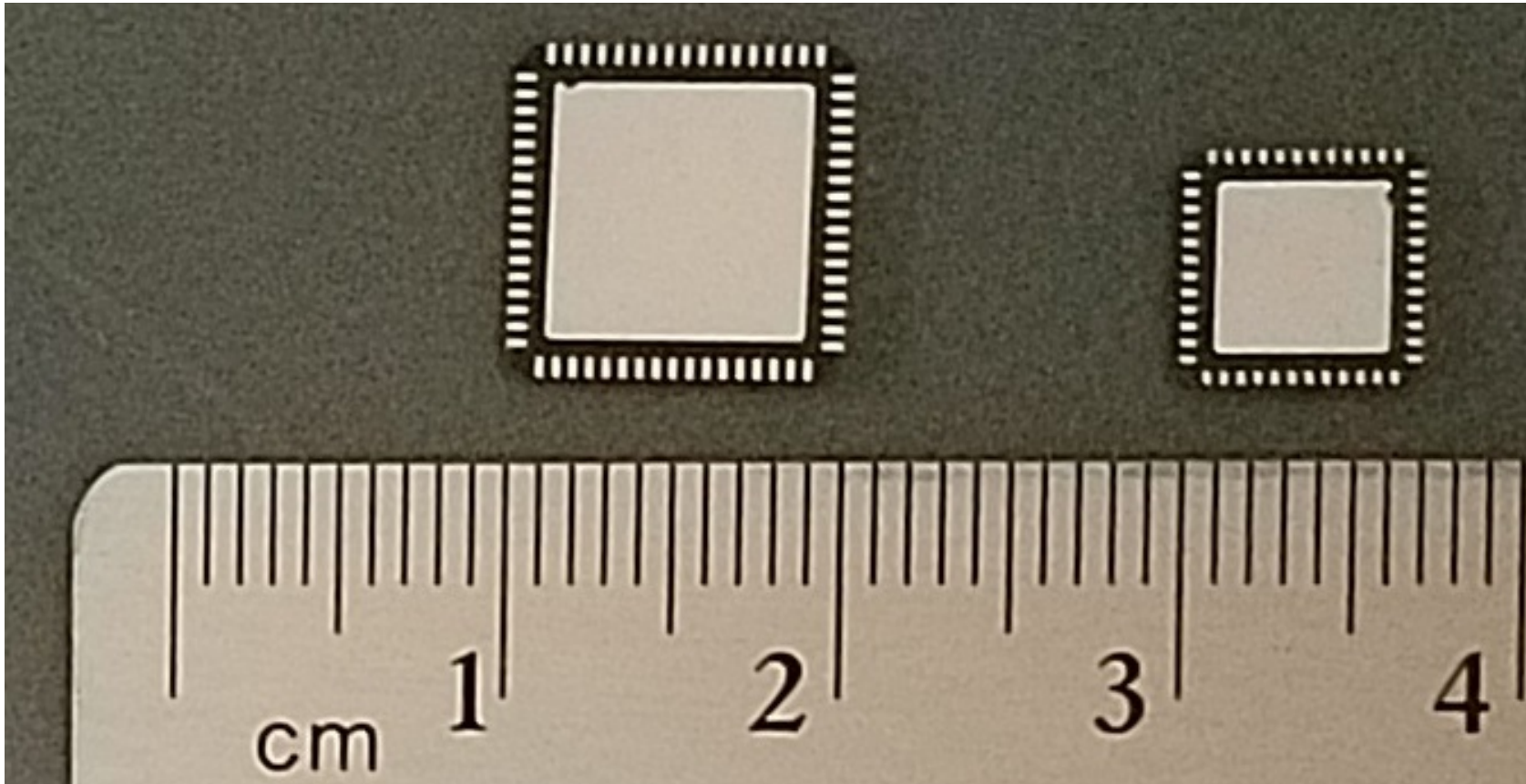
PR Test Board with a Solder Mask Tent on the Bottom Side

# METHODOLOGY – CIRCUIT BOARDS



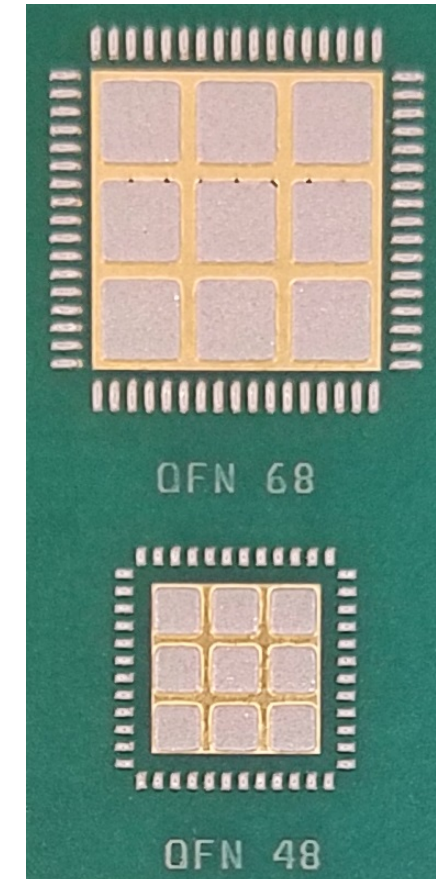
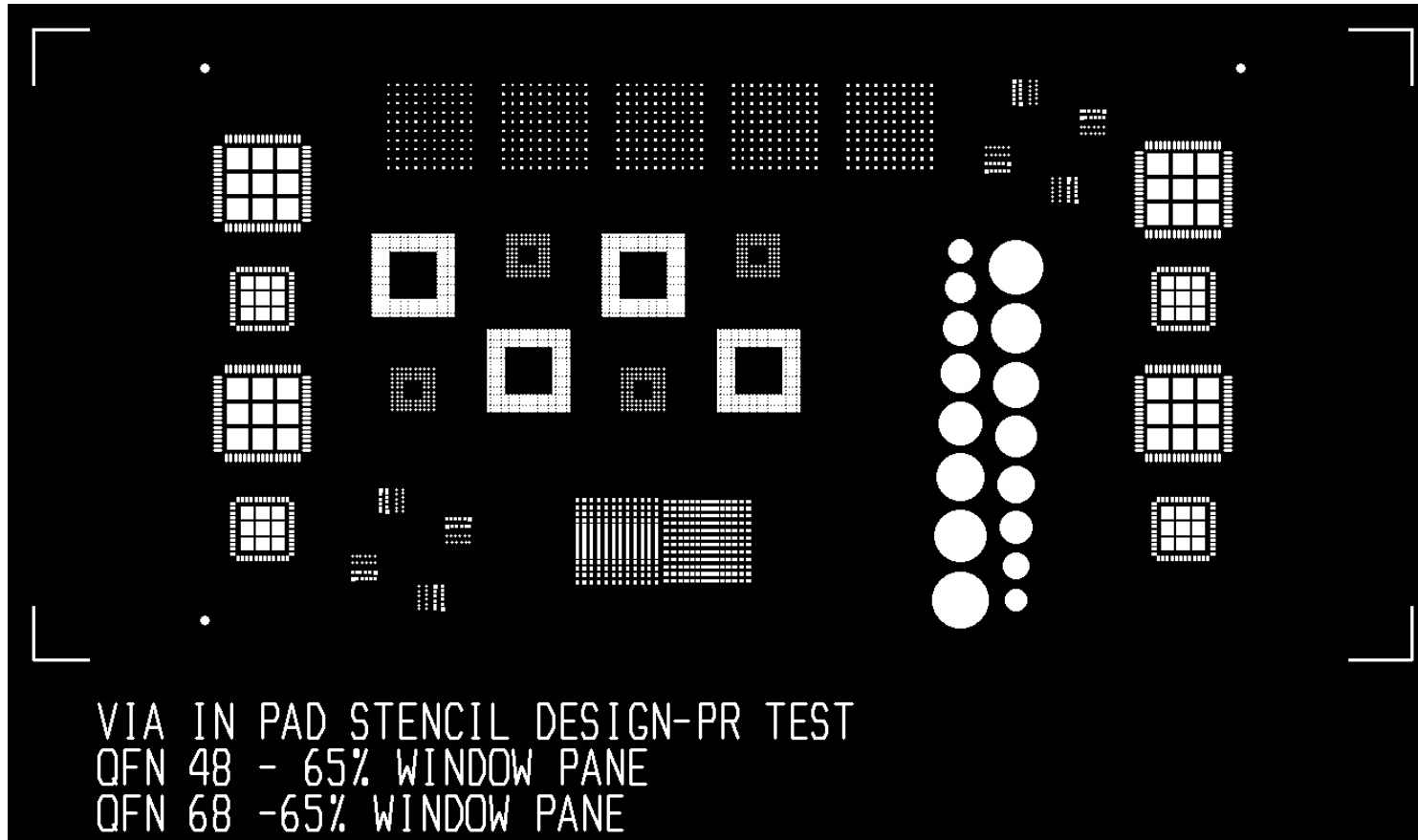
PR Test Board with Non-Conductive Via Fill, Plated with Cu and ENIG

## METHODOLOGY – QFN COMPONENTS



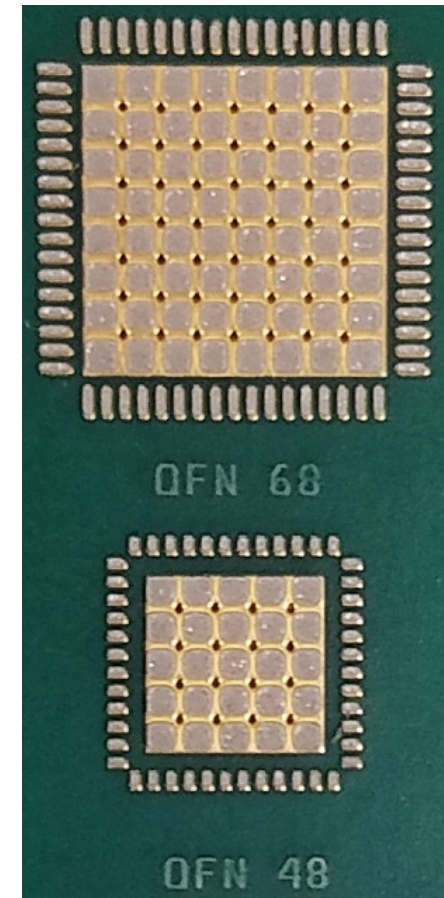
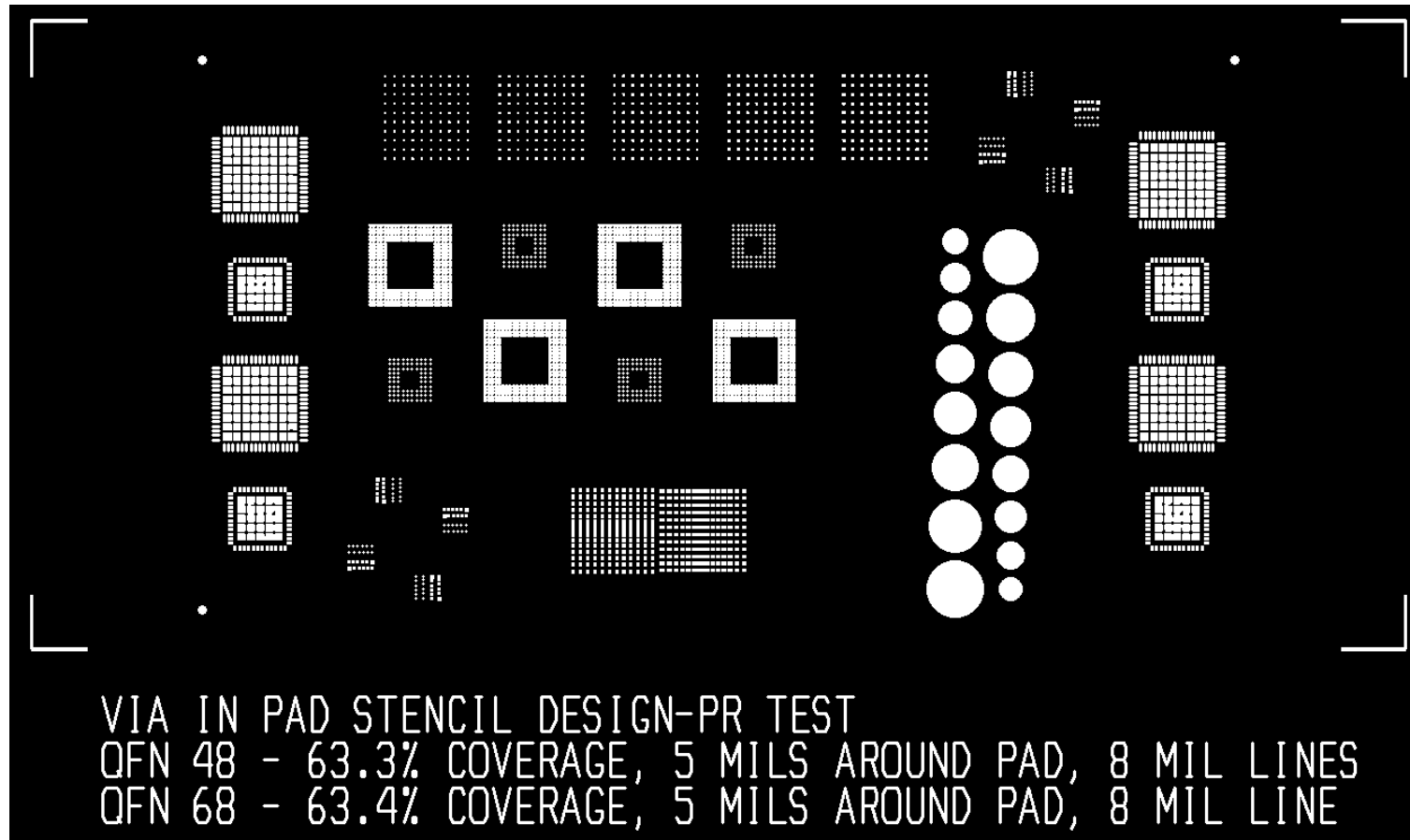
QFN Components: 10 mm body (68 lead) and 7 mm body (48 lead). Matte Tin Finish

## METHODOLOGY – STANDARD STENCIL



Standard Solder Paste Print: 65% Area Window Pane. Printed Over Via Holes

## METHODOLOGY – MODIFIED STENCIL

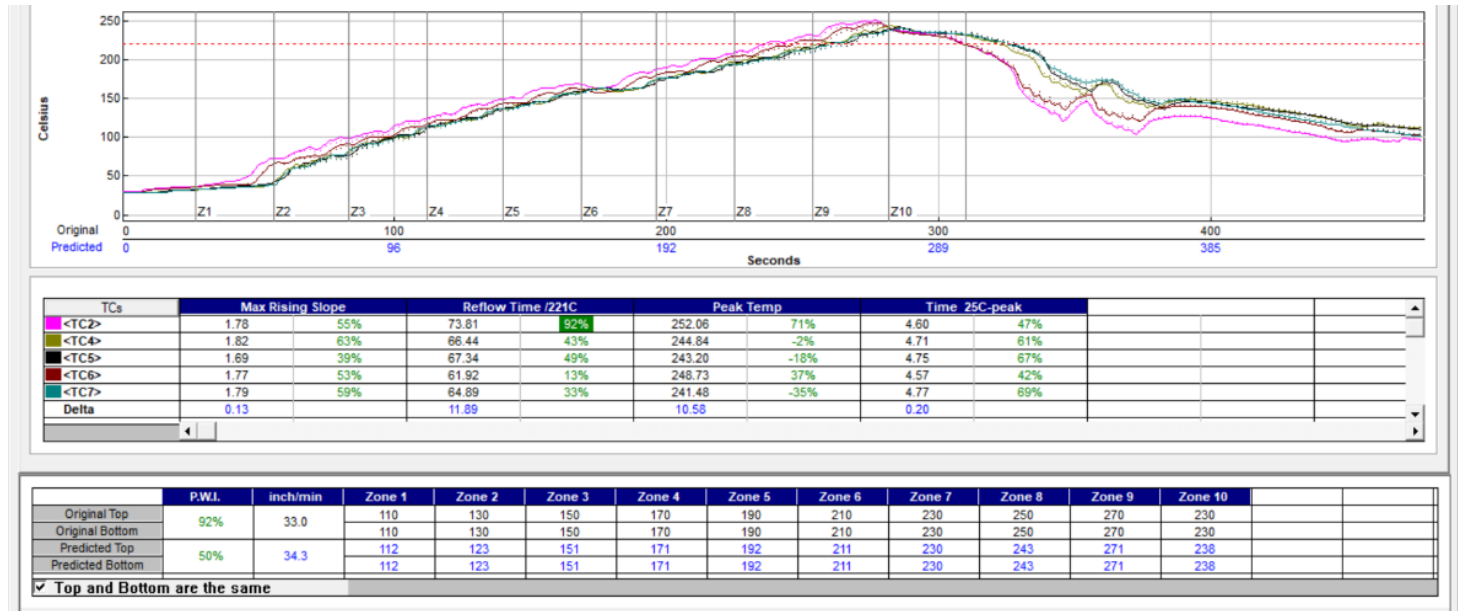


Modified Solder Paste Print: 63% Area Grid. Printed Around Via Holes

# METHODOLOGY – SOLDER PASTE AND REFLOW



No Clean SAC305 Type 3 Solder Paste



Setting	RTS Profile
Ramp rate	1.7 – 1.8 °C/sec
Reflow Time (> 220 °C)	61 – 67 sec
Peak temperature	241 to 248 °C
Profile length (25 °C to peak)	4.70 minutes

# METHODOLOGY – EXPERIMENTAL PROCEDURE

- 10 Circuit Boards For Each Variation
- 4 of Each QFN Size Placed and Boards were Reflowed
- Void Area and Largest Size Measured on Each QFN
- Images were Taken of Representative QFN Voiding
- Data was Analyzed and Statistics Generated



# VOIDING RESULTS



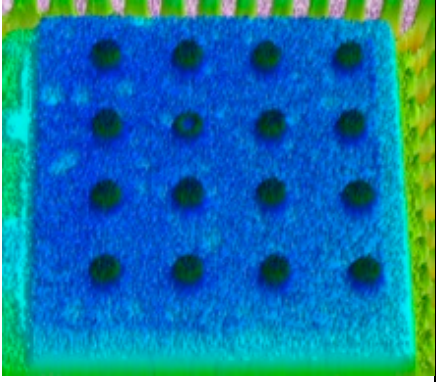
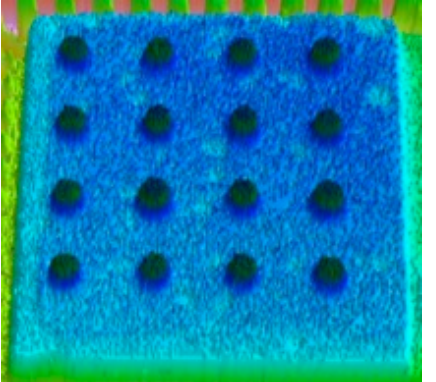
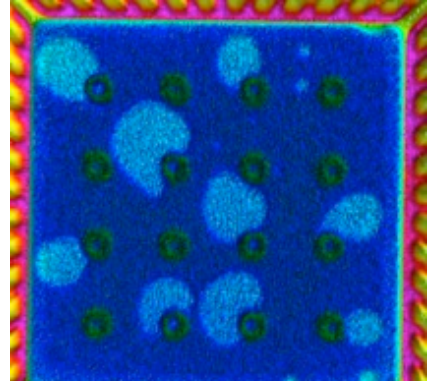
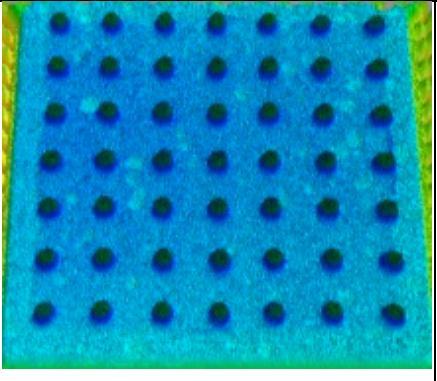
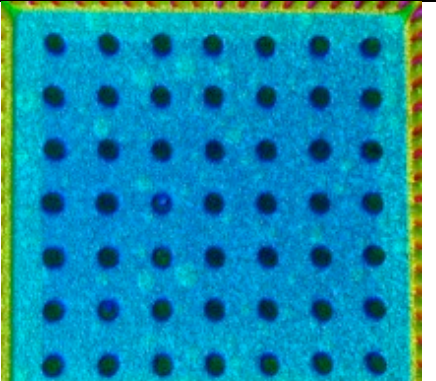
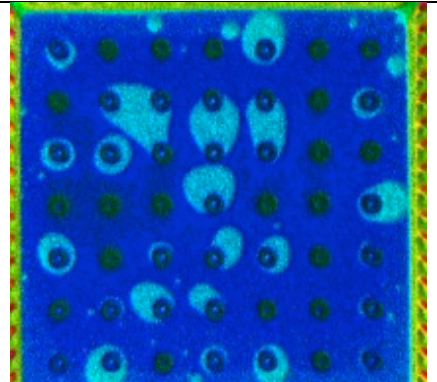


# VOIDING RESULTS – VIA FILL OPTIONS, STANDARD STENCIL

	Open Vias (No Fill)	Solder Mask Tent	Complete Plug	Flat Thermal Pad (No Via)
QFN7				
QFN10				

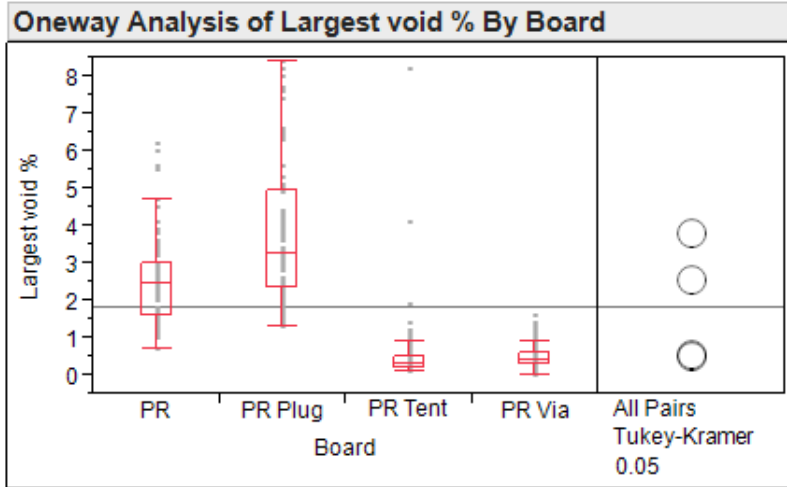
3D Voiding Images: Open Vias = Lower Voiding, Plugged and No Vias = More Voiding

# VOIDING RESULTS – VIA FILL OPTIONS, MODIFIED STENCIL

	Open Vias (No Fill)	Solder Mask Tent	Complete Plug
QFN7			
QFN10			

3D Voiding Images: Open Vias = Lower Voiding, Plugged Vias = More Voiding

# VOIDING SIZE – BY STENCIL



Excluded Rows 400

### Means Comparisons

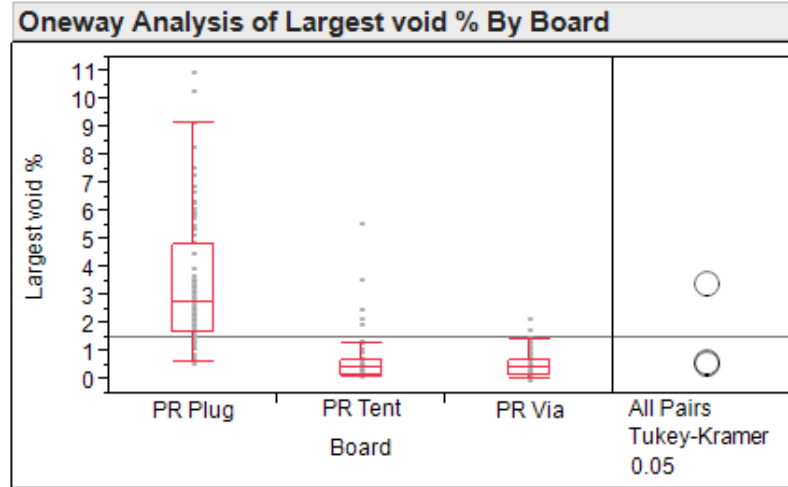
Comparisons for all pairs using Tukey-Kramer HSD

#### Connecting Letters Report

Level	Mean
PR Plug A	3.8162500
PR B	2.5537500
PR Tent C	0.5500000
PR Via C	0.4762500

Levels not connected by same letter are significantly different.

STANDARD STENCIL



Excluded Rows 480

### Means Comparisons

Comparisons for all pairs using Tukey-Kramer HSD

#### Connecting Letters Report

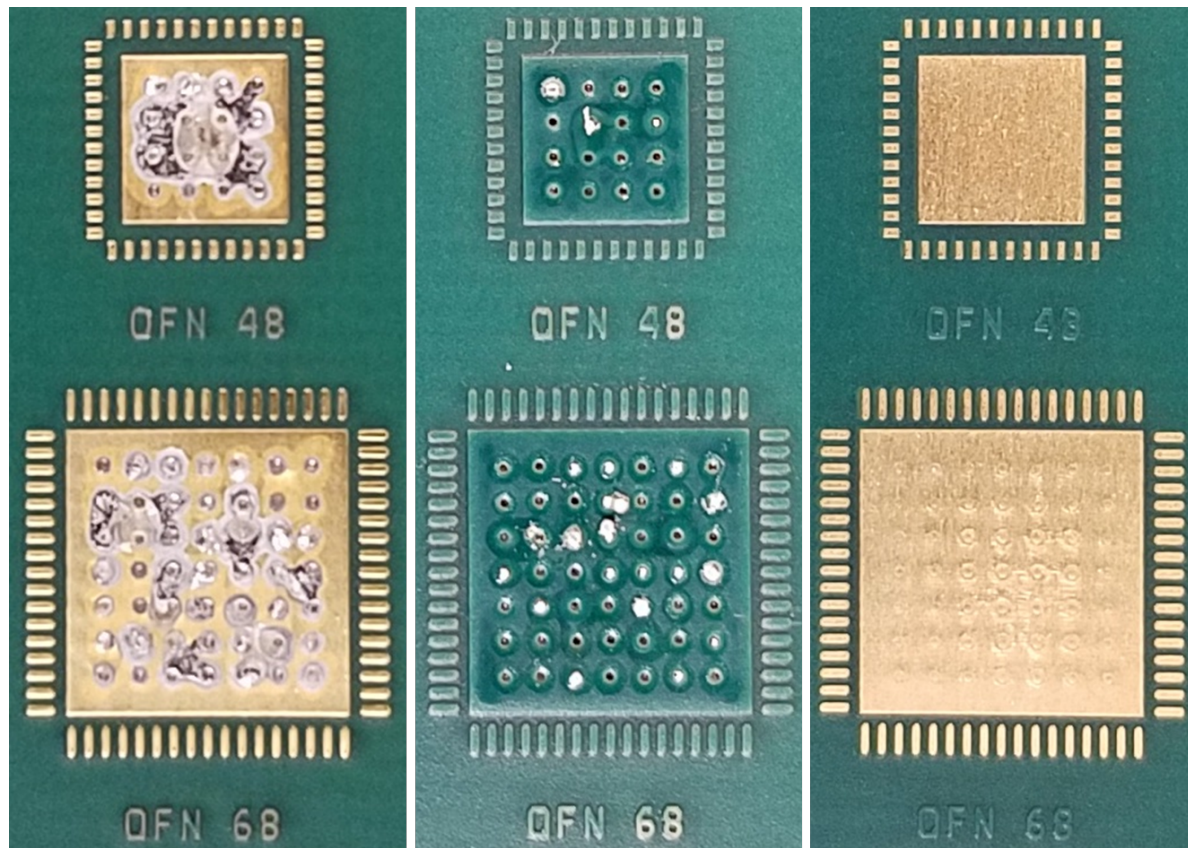
Level	Mean
PR Plug A	3.4425000
PR Tent B	0.6375000
PR Via B	0.5575000

Levels not connected by same letter are significantly different.

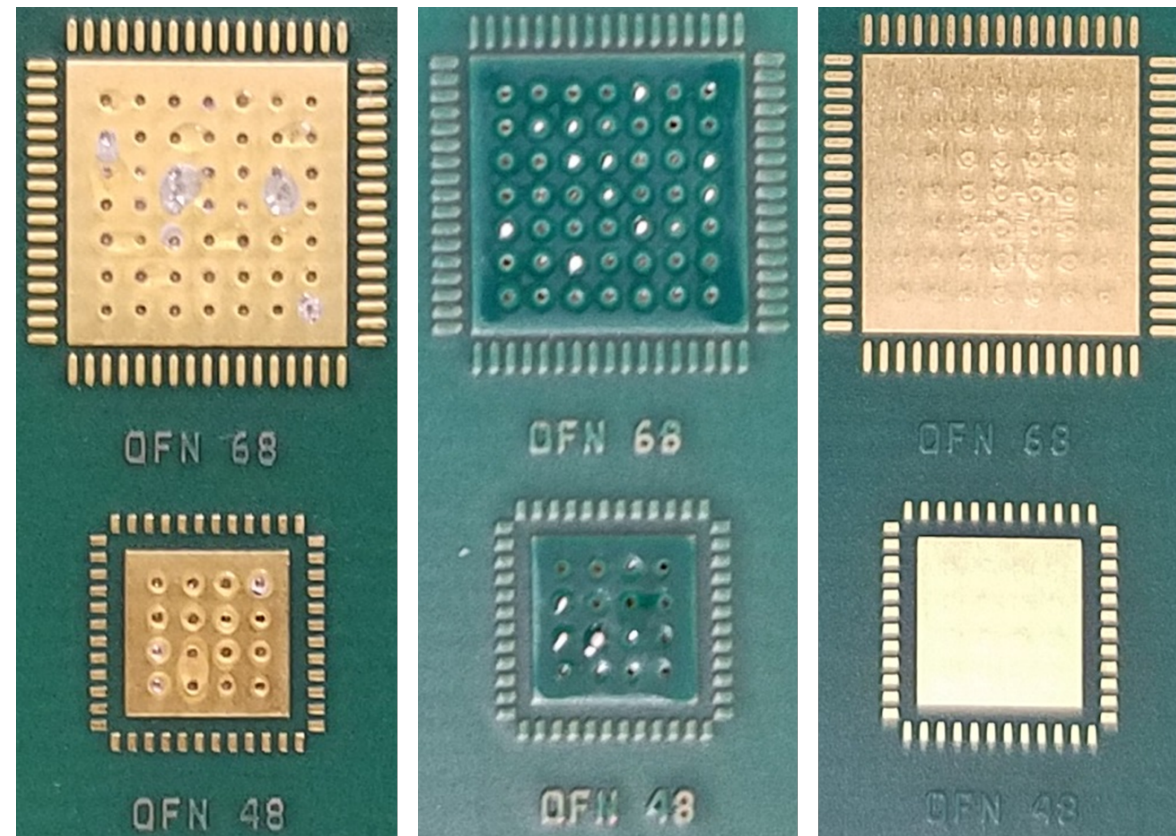
MODIFIED STENCIL

PR = Flat Pad (No Vias)  
 PR Plug = Plugged Vias  
 PR Tent = S/M Tented Vias  
 PR Via = Open Vias

## SOLDER FLOW TO THE BOTTOM OF THE BOARD



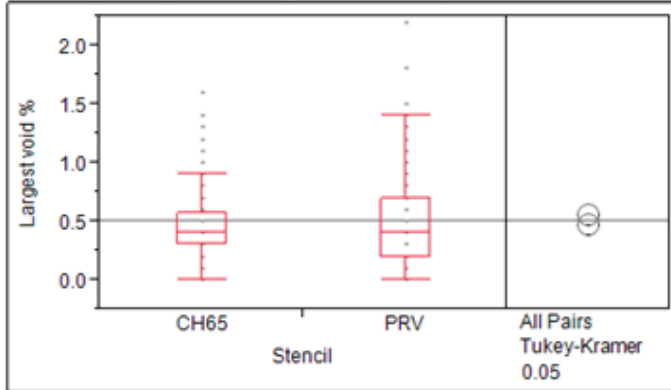
STANDARD STENCIL



MODIFIED STENCIL

# VOIDING SIZE BY STENCIL DESIGN FOR EACH VIA TYPE

Oneway Analysis of Largest void % By Stencil Board=PR Via



Excluded Rows 80

Means Comparisons

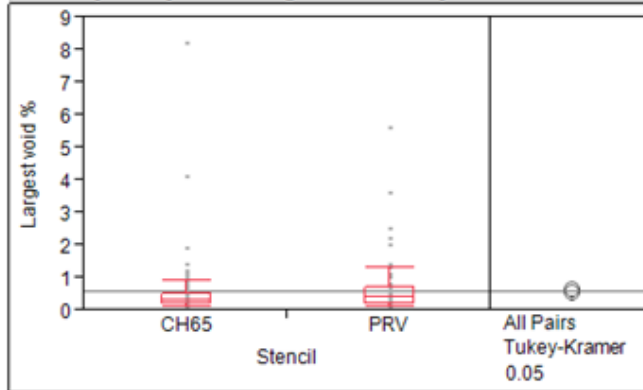
Comparisons for all pairs using Tukey-Kramer HSD

Connecting Letters Report

Level	Mean
PRV A	0.55750000
CH65 A	0.47625000

Levels not connected by same letter are significantly different.

Oneway Analysis of Largest void % By Stencil Board=PR Tent



Means Comparisons

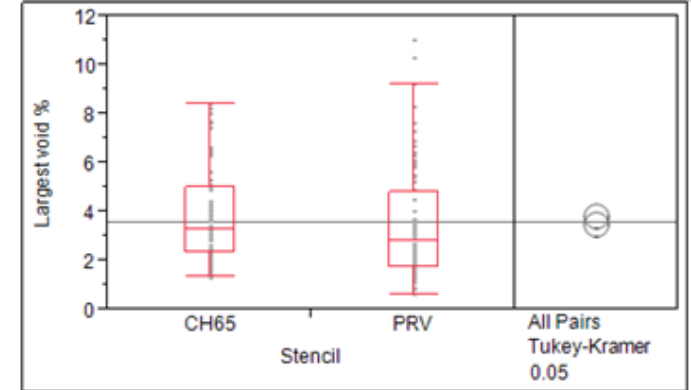
Comparisons for all pairs using Tukey-Kramer HSD

Connecting Letters Report

Level	Mean
PRV A	0.63750000
CH65 A	0.55000000

Levels not connected by same letter are significantly different.

Oneway Analysis of Largest void % By Stencil Board=PR Plug



Means Comparisons

Comparisons for all pairs using Tukey-Kramer HSD

Connecting Letters Report

Level	Mean
CH65 A	3.8162500
PRV A	3.4425000

Levels not connected by same letter are significantly different.

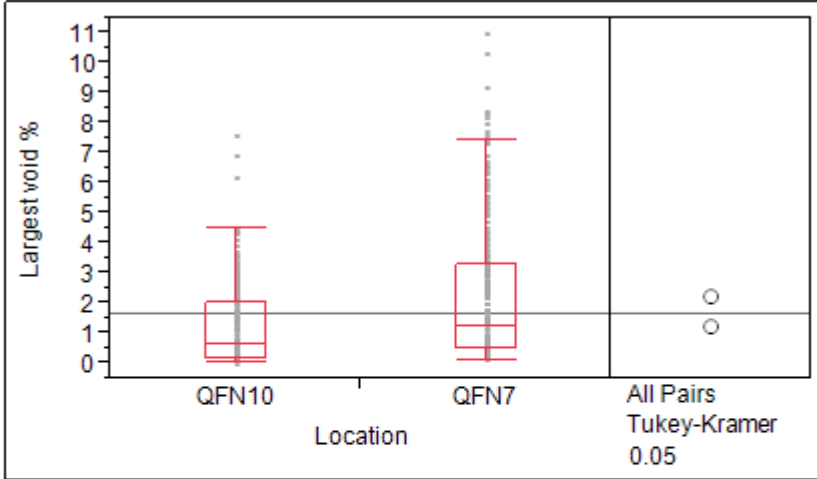
OPEN VIAS

TENTED VIAS

PLUGGED VIAS

# VOIDING BY QFN SIZE

Oneway Analysis of Largest void % By Location



Excluded Rows 160

**Means Comparisons**

Comparisons for all pairs using Tukey-Kramer HSD

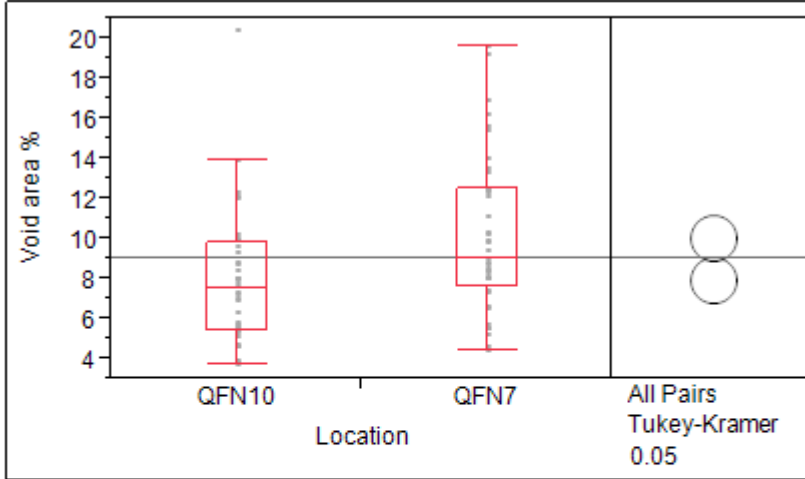
**Connecting Letters Report**

Level	Mean
QFN7 A	2.2310714
QFN10 B	1.2071429

Levels not connected by same letter are significantly different.

**LARGEST VOID SIZE**

Oneway Analysis of Void area % By Location



Excluded Rows 640

**Means Comparisons**

Comparisons for all pairs using Tukey-Kramer HSD

**Connecting Letters Report**

Level	Mean
QFN7 A	10.130000
QFN10 B	7.995000

Levels not connected by same letter are significantly different.

**VOID AREA**

Standard Stencil (65%)  
Flat QFN Pads – No Vias  
QFN10 Mass = 2x QFN7

# FILL THE VOID



## RECOMMENDATIONS TO FILL THE VOID

- Void size can be reduced using via holes in QFN thermal pads.
- Modifications to the stencil design limits the amount of solder flow through the via holes.
- Use of larger QFN's may reduce overall voiding.

**Via holes in QFN thermal pads certainly influence voiding!**



## FUTURE WORK

Work on mitigation strategies to reduce voiding is ongoing.  
Data will be presented at future technical conferences.



## ACKNOWLEDGEMENTS

Greg Smith with BlueRing Stencils designed and supplied the stencils used in this work.

**Thank You!**

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